YAMAHA® LSI

NO. 84-13 I

YM2203

FM Operator Type-N(OPN)

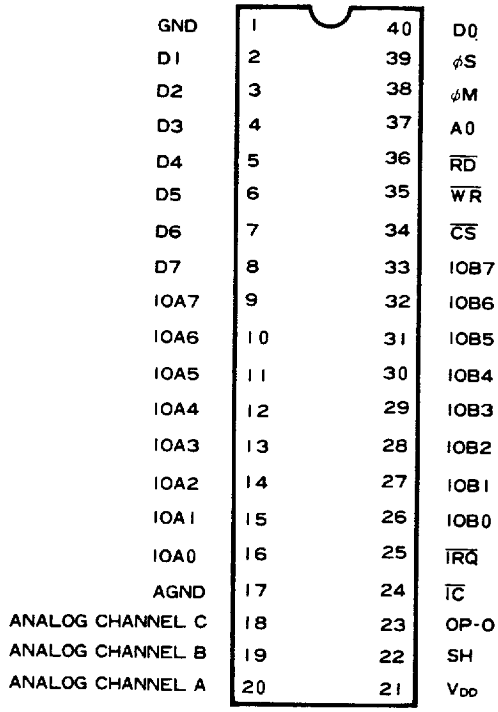
■ OUTLINE

OPN (FM OPERATOR TYPE-N) is a new type synthesizer which can produce all sounds required owing to the FM sound source system. It is provided with a built-in register which can store sound information and be connected easily with a microprocessor or microcomputer. It also comprises a square wave sound source different from the sound source according to the FM system and a noise generator.

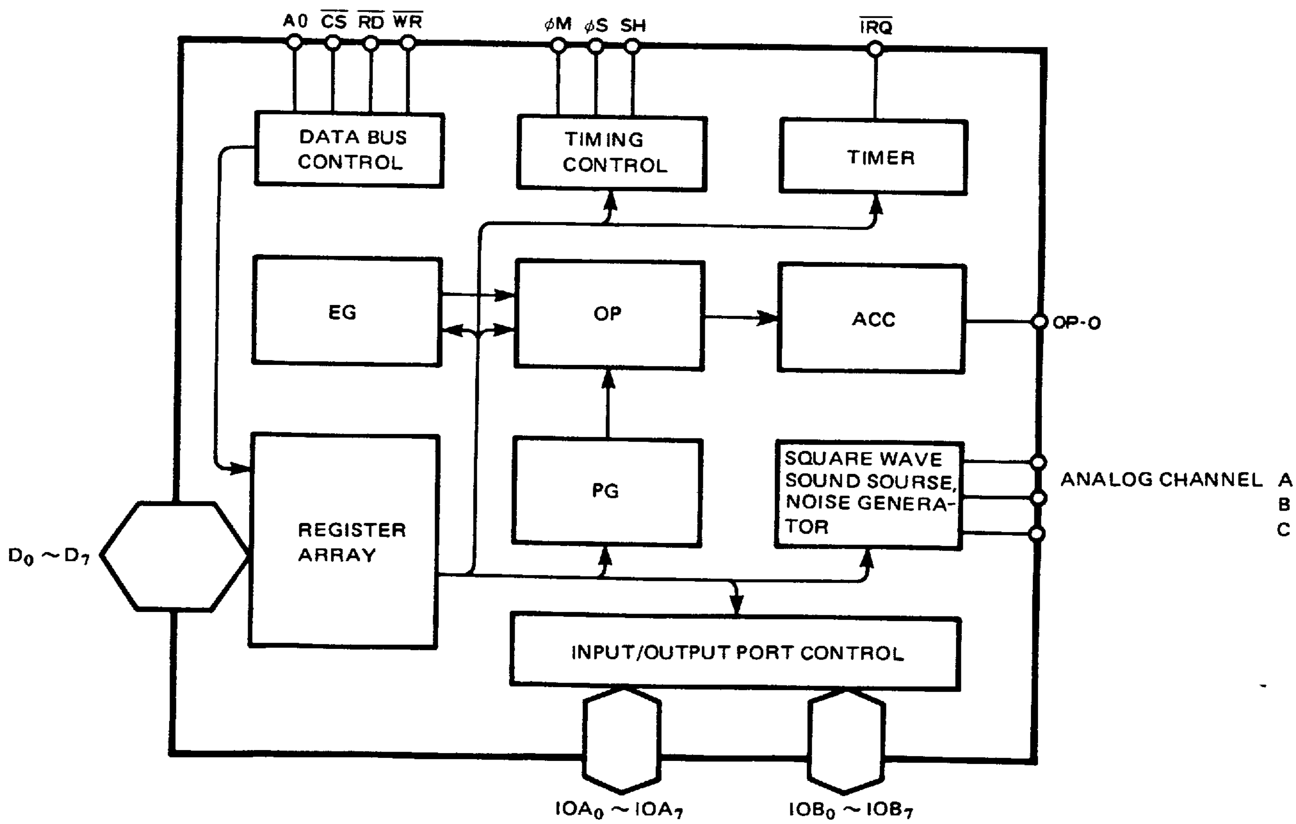
■ FEATURES

*The FM system sound source produce three different sounds simultaneously.
*One of the above three sounds can be set to the mode by which specific sound effects and composite sine wave sound are synthesized.
*Two programmable timers are incorporated.
*8 bits general purpose input/output ports of two system are incorporated.
*Three square wave sounds and white noise can be produced in addition to the FM system sounds.
*Clock divider is built in so that wide operating frequency range is obtained.
*Input and output are compatible with TTL.
*Nch-Si gate MOS LSI is used.
*Single phase power source of 5V is used.
*This is compatible with software of YM2149 and AY-3-8910 and 8912 produced by GI.

■ TERMINAL DIAGRAM



■ BLOCK DIAGRAM



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■ DESCRIPTION OF TERMINAL FUNCTION

1. **ϕM**

   This is the master clock of the OPN. The FM sound source and square wave sound source operate, based on this clock. The maximum input frequency up to 4.2MHz can be input by using a built-in 1/6 divider.

2. **ϕS · SH**

   These are the clock (ϕs) and the synchronous signal (SH). They drive a D/A converter which converts digital output of the FM sound source into analog output.

3. **D_0 through D_7**

   These 8-bit bi-directional bus exchange the data and address between the OPN and the microprocessor.

4. **$\overline{CS}$ · $\overline{RD}$ · $\overline{WR}$ · A_0**

   These signals control bi-directional bus of D_0 through D_7.

$\overline{CS}$ $\overline{RD}$ $\overline{WR}$ A_0	
0 1 0 0	Writes address into the register of the OPN.
0 1 0 1	Writes the resister content into the OPN.
0 0 1 0	Reads the OPN status.
0 0 1 1	Reads the content of the OPN register.
1 x x x	D_0 through D_7 bus line become high impedance.

* Read enable register addresses 00 througe 0F (16 bits).

5. **$\overline{IRQ}$**

   This is an interrupt signal sent from two timers. It can be masked by the program.

6. **$\overline{IC}$**

   This signal resets the system at low level. All the content of register array become "0".

7. **OP-O**

   This outputs the FM modulated audio signal as 13-bit serial data. Accordingly, an external D/A converter is necessary.

8. **Analog channel A, B and C**

   They are analog square wave audio signals. They can be mixed by setting resistance because of source follower.

9. **IOA_0 through IOA_7, IOB_0 through IOB_7**

   They are two sets of 8-bit input/output ports. Each terminal incorporates pull up resistance.

10. **AGND**

    This is analog ground terminal for the D/A converter which is built in the square wave sound source section.

11. **VDD**

    This is a power terminal of + 5V.

12. **GND**

    This is a ground terminal.

■ DESCRIPTION OF FUNCTIONS

The OPN is controlled based on the data written into the register. Accordingly, a microprocessor is free from the sound control operation except sending the data to the register.

The FM sound source determines a sound by the combination (modulation) of four sin waves. All the modulation systems such as feedback FM, simple FM and multiple FM are possible. In respect to the square wave sound source, this is compatible with YM2149 (SSG) and AY-3-8910 and 8912 (PSG.GI) in the use of the software. Therefore, function of the OPN can be improved by the exchange with the above LSI.

Each block of the OPN functions as follows.

*Envelope generator (EG): Determines the modulation index of the envelope and modulation wave of the FM sound source.

*Phase generator (PG): Determines the sin wave phase at each time step of the FM sound source.

*Operator (OP): Calculates the E sin θ value on the basis of the amplitude from the envelope generator and the phase from the phase generator.

*Accumulator (ACC): Accumulates and adds operator output of each channel to mix each sound of the FM sound source and matches with the D/A converter.

*Square wave sound source/noise generator:
Generates three different frequency square waves and pseudo-white noise. It can also mix noise and square wave. As for sound volume, it is possible to select either fixed sound volume (programmed value) or 10 pattern envelope producing mode. In this block, one D/A converter is provided for each sound.

*Input/output port control: These are the general-purpose input/output ports to gets interface with external equipment.

*Timer: Two types of timers are provided.

☆ Register content and address map

The OPN register is provided with the internal address as shown in the address map.

The content of each register (address) is as follows.

(1)	$ 00 ~ $ 05	Generates frequency of the square wave sound source.
(2)	$ 06	Generates frequency of noise source.
(3)	$ 07	Controls the input and output of the input and output ports and the output of musical sound and noise.
(4)	$ 08 ~ $ 0A	Controls sound volume. It is possible to select the fixed sound volume system (programmable) or the variable sound volume system.
(5)	$ 0B ~ $ 0C	Controls the envelope cycle in the variable sound volume sytem.
(6)	$ 0D	Specifies the envelope shape in the variable sound volume system.
(7)	$ 0E ~ $ 0F	8 bit general-purpose input and output ports.
(8)	$ 21	Test information, always set to "0".
(9)	$ 24 ~ $ 26	Gives the set time of Timers A and B.

(10)	\$ 27	Controls the operation of Timers A and B, and sets the third channel mode of the FM sound source.
(11)	\$ 2D ~ \$ 2F	Specifies the dividing number of the input clock. The dividing numbers 2 through 6 are for the FM sound source, and the numbers 1 through 4 are for square wave sound source.
(12)	\$ 30 ~ \$ 3E	Controls Detune and Multiple. This is used to set tones. This controls the relationship between the fundamental wave and harmonic.
(13)	\$ 40 ~ \$ 4E	Gives the total level. This information becomes the modulation index of the sound volume and modulation wave of the modulated wave.
(14)	\$ 50 ~ \$ 5E	Key -Scale controls the rate of change of A • D • S and R according to the keyboard information. Attack rate gives the rate of change of the envelope at the time of attack.
(15)	\$ 60 ~ \$ 6E	Decay Rate shows the rate of change of the envelope at the time of decay.
(16)	\$ 70 ~ \$ 7E	Sustain Rate shows the rate of change of the envelope at the time of sustain.
(17)	\$ 80 ~ \$ 8E	Sustain level shows the level of the shift from decay to sustain. Release rate shows the rate of change of the envelope at the time of release.
(18)	\$ 90 ~ \$ 9E	Generates the envelope including the repeat pattern similar to that of square wave sound source.
(19)	\$ A0 ~ \$ A6	Gives key-code (F-number) of each channel.
(20)	\$ A8 ~ \$ AE	Gives the key-code (F-number) of three channels when set to the special mode.
(21)	\$ B0 ~ \$ B2	Gives the modulation system (connection) of the FM modulation and the modulation factor of the feedback FM (self-feedback).

☆ FM system

In the FM system, musical sounds are synthesized by controlling various high harmonic waves by use of the frequency modulation.

The basic equation of the FM system is as follows.

$$F = A \sin (\omega Ct + I \sin \omega Mt) \qquad -(1)$$

Where A is output amplitude, I is modulation index, and ωC and ωM are angular frequencies of carrier and modulator, respectively.

This equation can also be expressed as follows.

$$\begin{aligned} F = A\,[&J_0 (I) \sin \omega Ct + J_1 (I) (\sin (\omega C + \omega M)t - \sin (\omega C - \omega M)t) \\ &+ J_2 (I) (\sin (\omega C + 2\omega M)t - \sin (\omega C - 2\omega M)t) \\ &+ \cdots\cdots\cdots \quad] \qquad -(2) \end{aligned}$$

Where, Jn (I) is the first class Bessel function of nth. As shown in the above equation, the FM system contains various harmonics and can control them.

The OPN provides the multiple FM modulation and feedback FM modulation shown in (3) and (4) in addition to the above FM modulation to produce every possible sound.

$$F = A \sin [\omega Ct + I_1 \sin (\omega M_1 t + I_2 \sin \omega M_2 t)] \qquad -(3)$$

$$F = A \sin (\omega Ct + \beta F) \qquad -(4)$$

* WRITE DATA

ADDRESS	DATA				COMMENT
21	TEST				LSI TEST DATA
24	TIMER-A				8 most significant bits of TIMER-A
25				TIMER -A	2 least significant bits of TIMER-A
26	TIMER-B				TIMER-B DATA
27	MODE	RESET B A	ENABLE B A	LOAD B A	TIMER-A/B control and 3 channel mode
28	SLOT			CH	Key-ON/OFF
2D					Set pre-scaler.
2E					Selection of the dividing numbers of 1/3 and 1/6.
2F					Set a divider to the dividing number of 1/2.
30 – 3E		DT	MULTI		Detune / Multiple (Addresses at 33, 37 and 3B are empty.)
40 – 4E		TL			Total Level (Addresses at 43, 47 and 4B are empty.)
50 – 5E	KS		AR		Key Scale / Attack Rate (Addresses at 53, 57 and 5B are empty.)
60 – 6E			DR		Decay Rate (Addresses at 63, 67 and 6B are empty.)
70 – 7E			SR		Sustain Rate (Addresses at 73, 77 and 7B are empty.)
80 – 8E	SL		RR		Sustain Level / Release Rate (Addresses at 83, 87 and 8B are empty.)
90 – 9E			SSG-EG		SSG-Type Envelop Control (Addresses at 93, 97 and 9B are empty.)
A0 A1 A2	F-Num. 1				F-Numbers / BLOCK
A4 A5 A6		BLOCK	F-Num. 2		
A8 A9 AA	3CH * F-Num. 1				3CH-3slot F-Numbers / BLOCK
AC AD AE		3CH * BLOCK	3CH * F-Num. 2		
B0 B1 B2		FB	CONNECT		Self-Feedback / Connection

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*READ / WRITE DATA

ADDRESS	DATA				COMMENT
00	Fine Tune				Channel-A Tone Period
01		Coarse Tune			
02	Fine Tune				Channel-B Tone Period
03		Coarse Tune			
04	Fine Tune				Channel-C Tone Deriod
05		Coarse Tune			
06		Period Control			Noise Period
07	IN/OUT IOB IOA	/Noise	/Tone		/ENABLE
08		M	Level		Channel-A Amplitude
09		M	Level		Channel-B Amplitude
0A		M	Level		Channel-C Amplitude
0B	Fine Tune				Envelop Period
0C	Coarse Tune				
0D		C	ATT	ALT HLD	Envelop Shape/Cycle
0E	I/O Port-A				I/O Port Date
0F	I/O Port-B				

*READ DATA

ADDRESS	DATA			COMMENT
xx	BUSY		FLAG B A	Status

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■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Rating

ITEM	RATING	UNIT
Terminal voltage	– 0.3 ~ 7.0	V
Ambient operating temperature	0 ~ 70	°C
Storage temperature	– 50 ~ 125	°C

2. Recommended Operation Conditions

ITEM	SYMBOL	MIN.	STD.	MAX.	UNIT
Supply voltage	VDD	4.75	5.0	5.25	V
	VSS	0	0	0	V

3. DC Characteristics

ITEM		SYMBOL	CONDITIONS	MIN.	STD.	MAX.	UNIT
Input high level voltage	Total input	VIH		2.0		VDD	V
Input low level voltage	Total input	VIL		– 0.3		0.8	V
Input leakage current	ϕM, $\overline{WR}$, $\overline{RD}$, A_0	IL	Vin = 0 ~ 5V	– 10		10	μA
Three-State (off) input current	D_0 ~ D_7	ITSL	Vin = 0 ~ 5V	– 10		10	μA
Output higl level voltage	Output except $\overline{IRQ}$	VOH_1 VOH_2	IOH_1 = 0.4mA IOM_2 = 40μA	2.4 3.3			V V
Output low level voltage	Total output	VOL	IOL = 2mA			0.4	V
Output leakage current (off)	$\overline{IRQ}$	IOL	VOH = 0 ~ 5V	– 10		10	μA
Analog output voltage	ANALOG-CHA, B, C	VOA	Max. Sound volume, no mixing	0.95		1.35	Vpp
Power current		IDD				120	mA
Pull-up resistance	IOA_0 ~ IOA_7, IOB_0 ~ IOB_7, $\overline{IC}$, $\overline{CS}$	RPU		60		600	kΩ
Input capacitance	Total input	C_1	f = 1MHz			10	pF
Output capacitance	Total output	C_0				10	pF

■ AC CHARACTERISTICS

4. AC Characteristics

ITEM		SYMBOL	CONDITIONS	MIN.	STD.	MAX.	UNIT
Input clock frequency	ϕM	fc	Pre-scaler function (Fig. A-1)	0.7		4.2	MHz
Input clock duty	ϕM			40	50	60	%
Input clock rise time	ϕM	TR	(Fig. A-1)			50	ns
Input clock breaking time	ϕM	TF	(Fig. A-1)			50	ns

Access to FM sound source

ITEM		SYMBOL	CONDITIONS	MIN.	STD.	MAX.	UNIT
Address set-up time	A_0	TAS	(Figs. A-2 and A-3)	10			ns
Address hold time	A_0	TAH	(Figs. A-2 and A-3)	10			ns
Chip select write width	$\overline{CS}$	TCSW	(Fig. A-2)	200			ns
Chip select read width	$\overline{CS}$	TCSR	(Fig. A-3)	250			ns
Write pulse write width	$\overline{WR}$	TWW	(Fig. A-2)	200			ns
Write data set-up time	$D_0 \sim D_7$	TWDS	(Fig. A-2)	100			ns
Write data hold time	$D_0 \sim D_7$	TWDH	(Fig. A-3)	20			ns
Read pulse width	$\overline{RD}$	TRW	(Fig. A-3)	250			ns
Read data access time	$D_0 \sim D_7$	TACC	CL = 100pF (Fig. A-3)			250	ns
Read data hold time	$D_0 \sim D_7$	TRDH	(Fig. A-3)	10			ns
Output rise time	ϕs	TOR_1	CL = 100pF (Fig. A-4)			200	ns
	OP–O, SH	TOR_2	CL = 100 pF (Fig. A-5)			300	ns
Output rise time	ϕs	TOF_1	CL = 100pF (Fig. A-4)			200	ns
	OP–O, SH	TOF_2	CL = 100pF (Fig. A-5)			300	ns

Access to SSG sound sourse

ITEM		SYMBOL	CONDITIONS	MIN.	STD.	MAX.	UNIT
Address set-up time	A_0	TSAS	(Figs. A-7 and A-8)	10			ns
Address hold time	A_0	TSAH	(Figs. A-7 and A-8)	10			ns
Chip select writh width	$\overline{CS}$	TSCSW	(Fig. A-7)	250			ns
Chip select read width	$\overline{CS}$	TSCSR	(Fig. A-8)	400			ns
Write pulse write width	$\overline{WR}$	TSWW	(Fig. A-7)	250			ns
Write data set-up time	$D_0 \sim D_7$	TSWDS	(Fig. A-7)	0			ns
Write data hold time	$D_0 \sim D_7$	TSWDH	(Fig. A-7)	20			ns
Read pulse width	$\overline{RD}$	TSRW	(Fig. A-8)	400			ns
Read data access time	$D_0 \sim D_7$	TSACC	CL = 100pF (Fig. A-8)			400	ns
Read data hold time	$D_0 \sim D_7$	TSRDH	(Fig. A-8)	10			ns

ITEM		SYMBOL	CONDITIONS	MIN.	STD.	MAX.	UNIT
Reset pulse width	$\overline{IC}$	TICW	(Fig. A-9)	72*			cycle

* Depends on the dividing number of prescaler.
Pulse width = (dividing number) x 12

■ TIMING DIAGRAM (Timing is set on the basis of the values: V_{IH} = 2.0V and V_{IL} = 0.8V.)

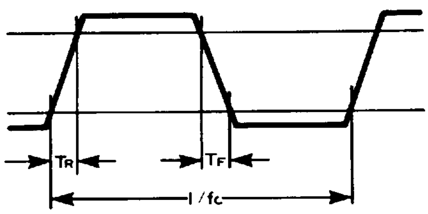

Fig. A-1 Clock timing

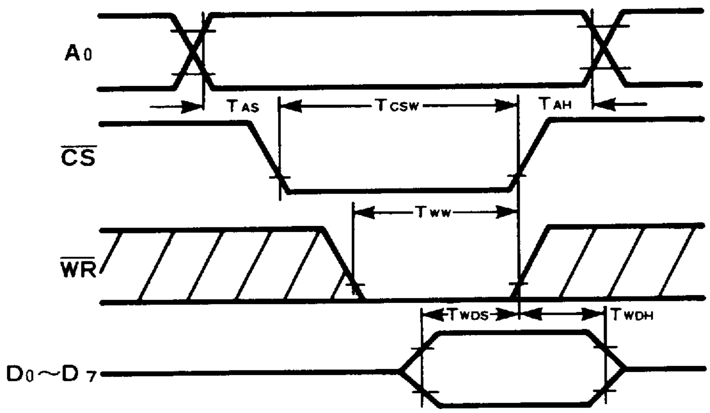

Fig. A-2 FM section write timing

Note.
T_{CSW}, T_{WW} and T_{WDH} are determined based on the time when either $\overline{CS}$ or $\overline{WR}$ goes to the high level.

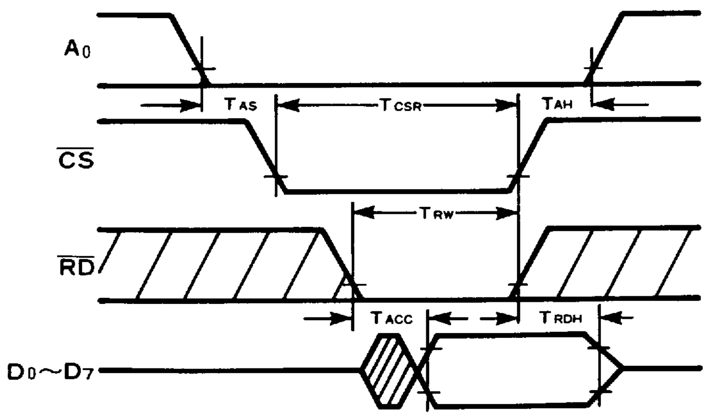

Fig. A-3 FM section read timing

Note.
T_{AAC} is determined based on the time when either $\overline{CS}$ or $\overline{RD}$ goes to the low level. T_{CSR}, T_{RW} and T_{RDH} are determined based on the time when either $\overline{CS}$ or $\overline{RD}$ goes to the high level.

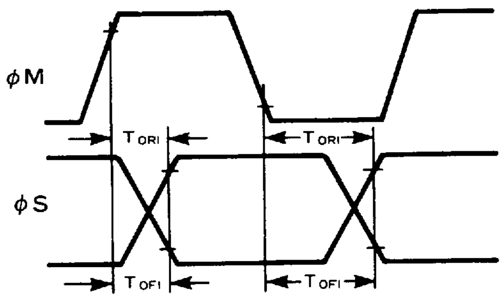

Fig. A-4-a φM and φS
(dividing numbers: 2 and 3)

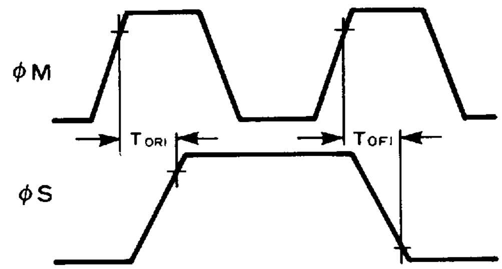

Fig. A-4-b φM and φS
(dividing number: 6)

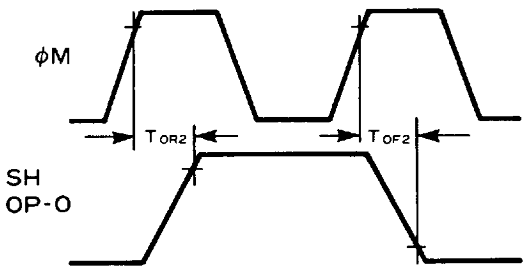

Fig. A-5 φM and SH · OP-O

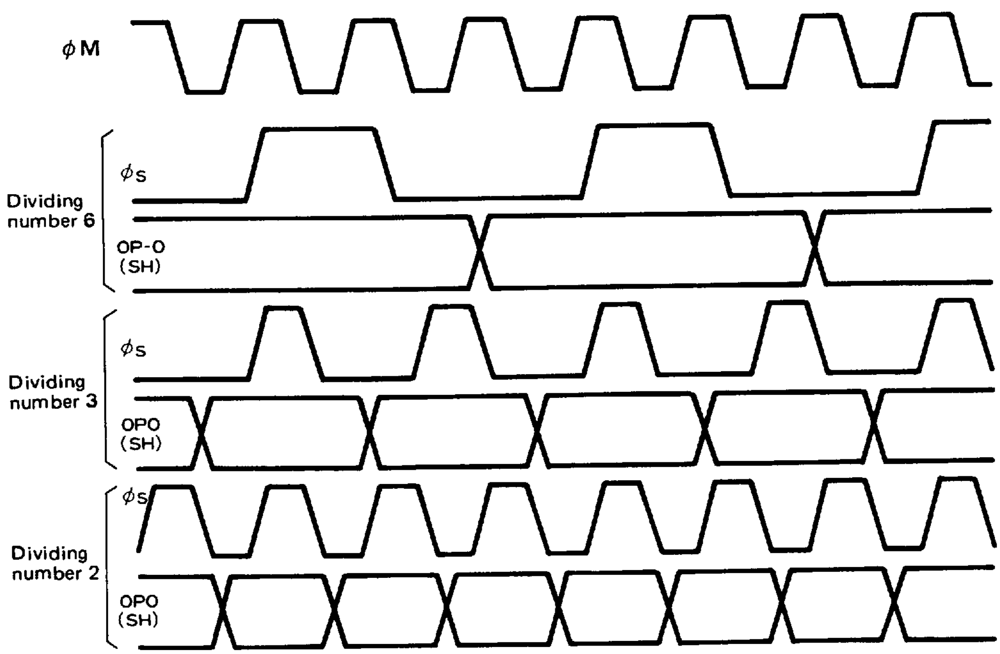

Fig. A-6 Timing of φs and OP-O/CH at each dividing number

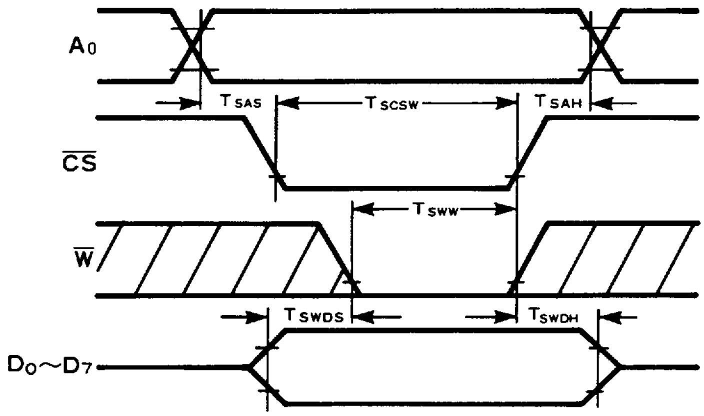

Fig. 6-7 SSG section write timing

Note.
TSWDS is determined based on the time when either $\overline{CS}$ or $\overline{WR}$ goes to the low level.
TSCW , TSWW and TSWDH are determined based on the time when either $\overline{CS}$ or $\overline{WR}$ goes to the High level.

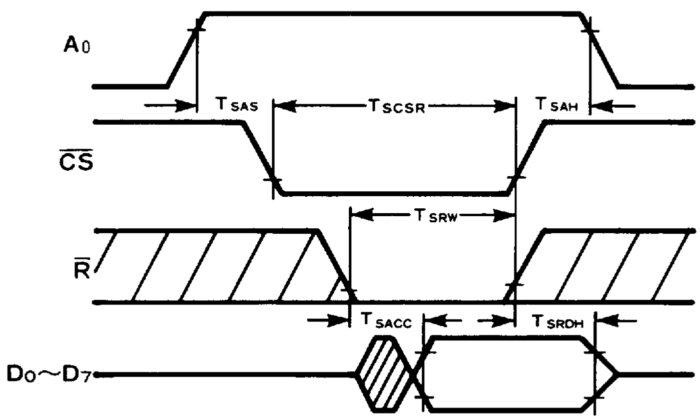

Fig. A-8 SSG section read timing

Note.
TSACC is determined based on the time when either $\overline{CS}$ or $\overline{RD}$ goes to the low level. TSCSR , TSRW and TSRDH are determined based on the time when either $\overline{CS}$ or $\overline{RD}$ goes to the High level.

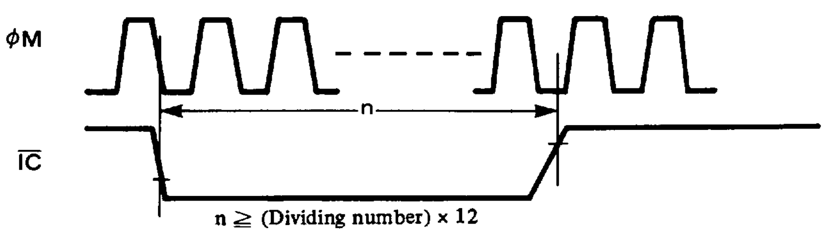

Fig. A-9 Reset pulse

■ OUTER DIMENSION DRAWING