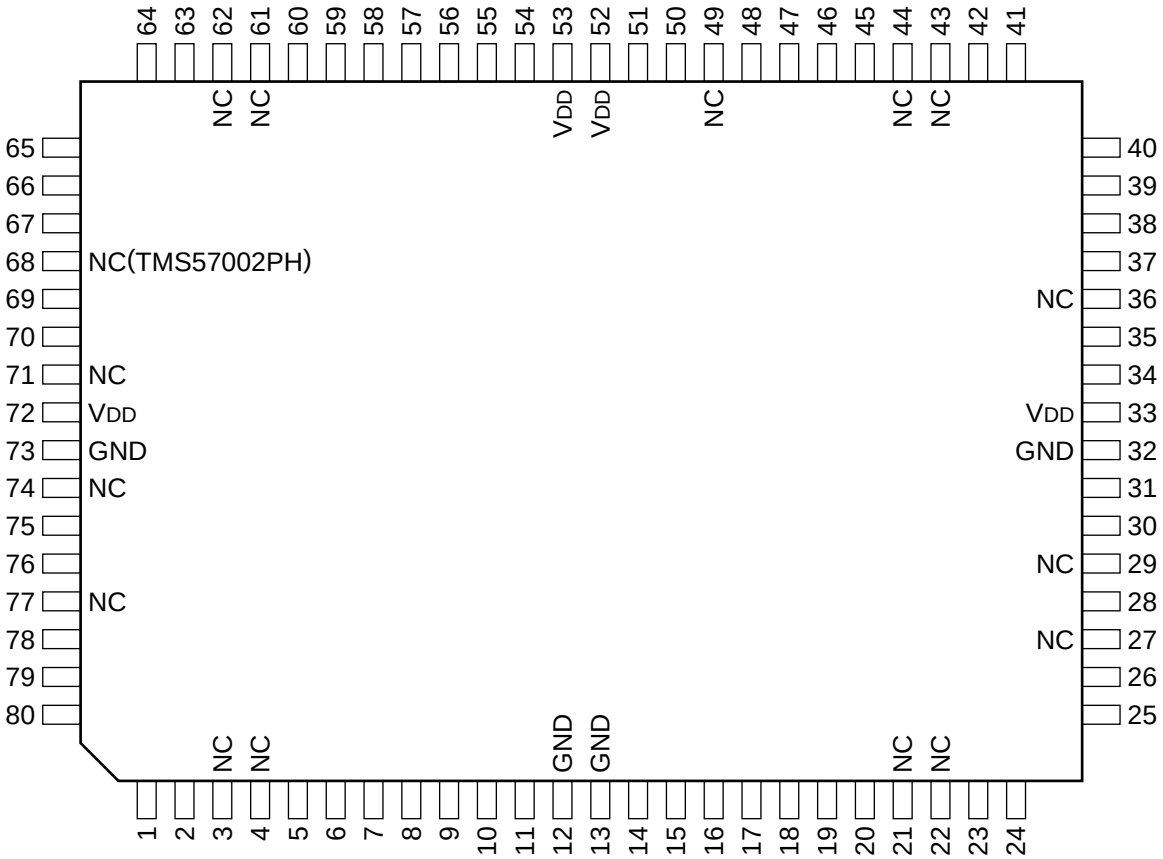
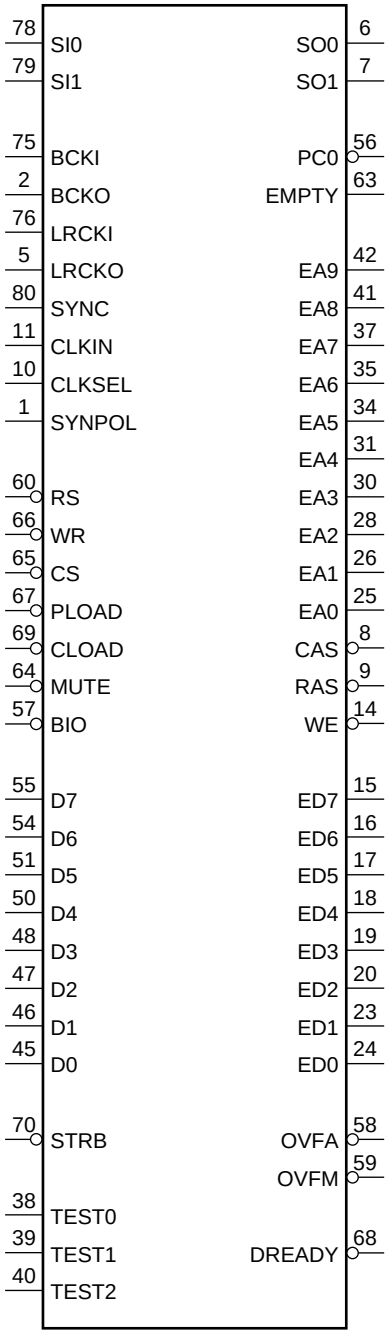
C-MOS DIGITAL AUDIO SIGNAL PROCESSOR

—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I	SYNPOL	21	—	NC	41	O	EA8	61	—	NC
2	I	BCKO	22	—	NC	42	O	EA9 (MSB)	62	—	NC
3	—	NC	23	I/O	ED6	43	—	NC	63	O	EMPTY
4	—	NC	24	I/O	ED7 (MSB)	44	—	NC	64	I	$\overline{\text{MUTE}}$
5	I	LRCKO	25	O	EA0 (LSB)	45	I	D0 (LSB)	65	I	$\overline{\text{CS}}$
6	O	SO0	26	O	EA1	46	I	D1	66	I	$\overline{\text{WR}}$
7	O	SO1	27	—	NC	47	I	D2	67	I	$\overline{\text{PLOAD}}$
8	O	$\overline{\text{CAS}}$	28	O	EA2	48	I	D3	68	O	NC/$\overline{\text{DREADY}}$*
9	O	$\overline{\text{RAS}}$	29	—	NC	49	—	NC	69	I	$\overline{\text{CLOAD}}$
10	I	CLKSEL	30	O	EA3	50	I	D4	70	I	$\overline{\text{STRB}}$
11	I	CLKIN	31	O	EA4	51	I	D5	71	—	NC
12	—	GND	32	—	GND	52	—	VDD	72	—	VDD
13	—	GND	33	—	VDD	53	—	VDD	73	—	GND
14	O	$\overline{\text{WE}}$	34	O	EA5	54	I	D6	74	—	NC
15	I/O	ED0 (LSB)	35	O	EA6	55	I	D7 (MSB)	75	I	BCKI
16	I/O	ED1	36	—	NC	56	O	$\overline{\text{PC0}}$	76	I	LRCKI
17	I/O	ED2	37	O	EA7	57	I	$\overline{\text{BIO}}$	77	—	NC
18	I/O	ED3	38	I	TEST0	58	O	$\overline{\text{OVFA}}$	78	I	SI0
19	I/O	ED4	39	I	TEST1	59	O	$\overline{\text{OVFM}}$	79	I	SI1
20	I/O	ED5	40	I	TEST2	60	I	$\overline{\text{RS}}$	80	I	SYNC

* : TMS57002PH ; NC.



INPUT

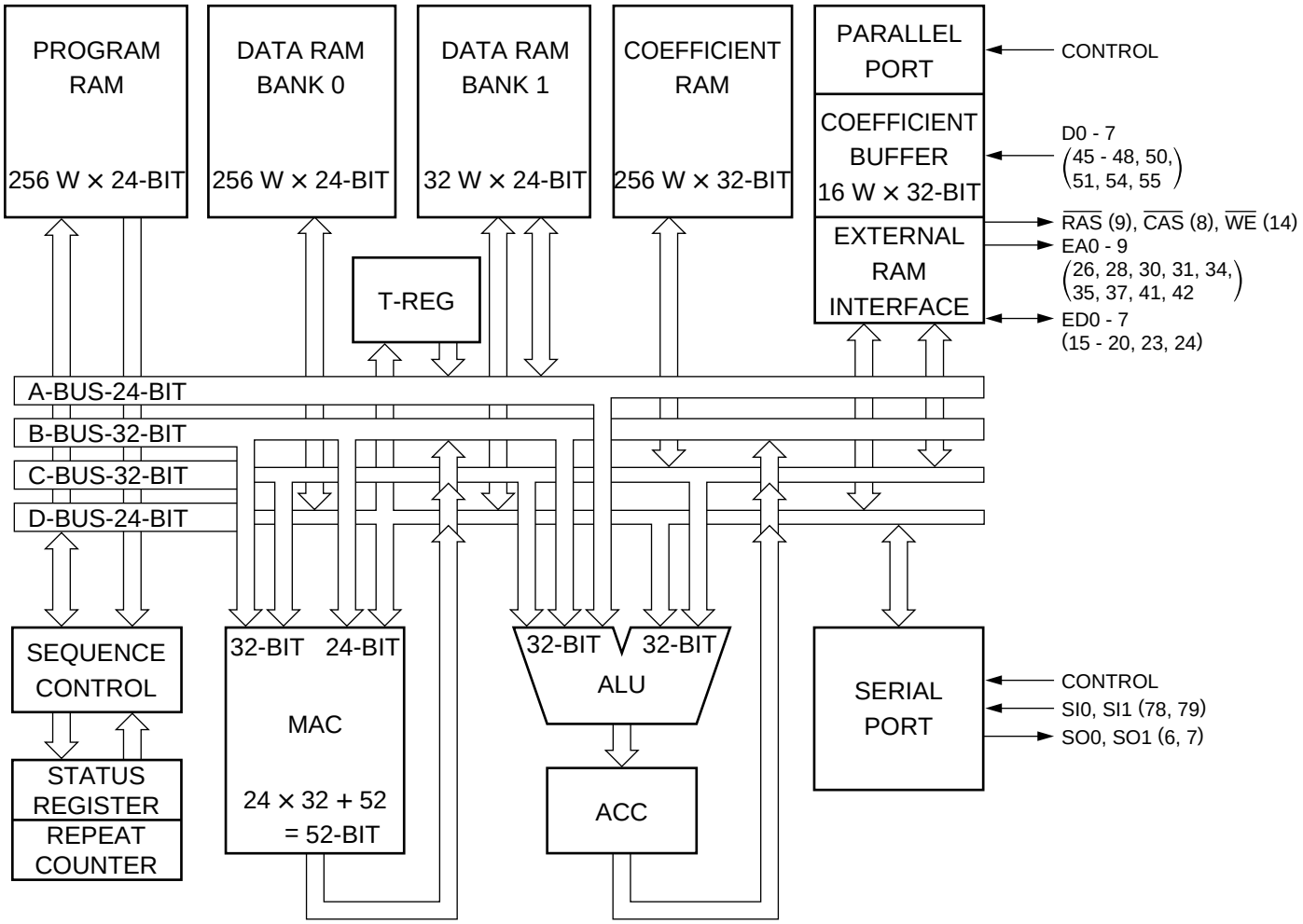
BCKI	;	BIT CLOCK FOR SERIAL INPUT
BCKO	;	BIT CLOCK FOR SERIAL OUTPUT
$\overline{BIO}$	;	BRANCH CONTROL
CLKIN	;	MASTER CLOCK
CLKSEL	;	CLKIN FREQUENCY SELECT (L ; 512 fs H ; 256 fs)
$\overline{CLOAD}$	;	COUNTING LOAD
$\overline{CS}$	;	CHIP ENABLE FOR PARALLEL PORT
D0 - 7	;	PARALLEL PORT
$\overline{DREADY}$	;	DATA READY SIGNAL TO HOST CONTROLLER
LRCKI	;	RIGHT AND LEFT CHANNEL THRESHOLD CLOCK FOR SERIAL INPUT
LRCKO	;	RIGHT AND LEFT CHANNEL THRESHOLD CLOCK FOR SERIAL OUTPUT
$\overline{MUTE}$	;	MUTE
$\overline{PLOAD}$	;	PROGRAM LOAD
$\overline{RS}$	;	RESET (L ; RESET H ; NORMAL OPERATION)
SI0, 1	;	SERIAL INPUT DATA 0, 1
$\overline{STRB}$	;	DATA STROBE FOR PARALLEL PORT
SYNC	;	PROGRAM SYNC SIGNAL
SYNPOL	;	SYNC SIGNAL EFFECTIVE EDGE SELECT (L ; DOWN H ; UP)
TEST0 - 2	;	FOR TEST
$\overline{WR}$	;	RIGHT ENABLE FOR PARALLEL PORT

OUTPUT

$\overline{CAS}$	;	COL ADDRESS STROBE FOR OUTER EXTERNAL RAM
EA0 - 9	;	OUTER EXTERNAL RAM ADDRESS
EMPTY	;	COUNTING BUFFER EMPTY
$\overline{OVFA}$	;	ALU OVERFLOW FLAG (OPEN DRAIN OUTPUT)
$\overline{OVFM}$	;	MAC OVERFLOW FLAG (OPEN DRAIN OUTPUT)
PC0	;	PROGRAM COUNTER 0
$\overline{RAS}$	;	ROW ADDRESS STROBE FOR OUTER EXTERNAL RAM
SO0, 1	;	SERIAL OUTPUT DATA 0, 1
$\overline{WE}$	;	RIGHT ENABLE FOR OUTER EXTERNAL RAM

INPUT/OUTPUT

ED0 - 7	;	OUTER EXTERNAL RAM DATA


PROGRAM RAM
256 W × 24-BIT
DATA RAM BANK 0
256 W × 24-BIT
DATA RAM BANK 1
32 W × 24-BIT
COEFFICIENT RAM
256 W × 32-BIT
PARALLEL PORT
CONTROL
COEFFICIENT BUFFER
16 W × 32-BIT
D0 - 7
(45 - 48, 50, 51, 54, 55)
EXTERNAL RAM INTERFACE
RAS (9), CAS (8), WE (14)
EA0 - 9
(26, 28, 30, 31, 34, 35, 37, 41, 42)
ED0 - 7
(15 - 20, 23, 24)
T-REG
A-BUS-24-BIT
B-BUS-32-BIT
C-BUS-32-BIT
D-BUS-24-BIT
SEQUENCE CONTROL
STATUS REGISTER
REPEAT COUNTER
32-BIT 24-BIT
MAC
24 × 32 + 52
= 52-BIT
32-BIT 32-BIT
ALU
ACC
SERIAL PORT
CONTROL
SI0, SI1 (78, 79)
SO0, SO1 (6, 7)